REMARKS

Claims 1-31 are pending in the present application.

Claims 1-31 stand rejected under 35 U.S.C. §102(e) as being anticipated by Miller (U.S. Patent Number 6,604,161). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites

> "An input/output node switch for a multiprocessor computer system, said input/output node switch comprising:
>
> a bridge unit implemented on an integrated circuit chip coupled to receive a plurality of peripheral transactions from a peripheral bus and configured to transmit a plurality of upstream packet transactions corresponding to said plurality of peripheral transactions;
>
> a packet bus switch unit implemented on said integrated circuit chip coupled to receive said plurality of upstream packet transactions on an internal point-to-point packet bus link and configured to determine a destination of each of said plurality of upstream packet transactions;
>
> wherein said packet bus switch unit is further configured to route selected ones of said plurality of upstream packet transactions to **a first processor interface** coupled to **a first point-to-point packet bus link** and to route others of said plurality of upstream packet transactions to **a second processor interface** coupled to **a second point-to-point packet bus link** in response to determining said destination each of said plurality of upstream packet transactions." (Emphasis added)

The Examiner asserts that Miller teaches in FIG. 1 a bridge unit 130 delivering packets to each of CPUs accordingly based on each CPUs addresses. The Applicant respectfully disagrees with the Examiner's assertion.

Specifically, in FIG. 1, Miller shows a bridge unit connected directly to a memory controller 160. It is the memory controller that is connected to the CPUs. Furthermore, Miller teaches at col. 4, lines 18-20 "Bridge device 130 encodes the interrupt with source and destination information. Then the bridge device 130 sends an interrupt write packet.

The interrupt write packet is transmitted to CPU 170 **through a memory controller 160** to launch an interrupt routine." (Emphasis added)

From the foregoing, it appears that Miller is teaching a PCI bus bridge that packetizes PCI interrupts into interrupt write packets (i.e. creates interrupt write packets encoded with source and destination information) and **sends those packets to a memory controller via a single packet based interconnect**. Miller is silent on how the memory controller routes the packets to the CPUs, and thus does not teach more than one packet based interconnect.

Thus, Applicant respectfully submits that Miller does not teach or disclose each and every element recited in Applicant's claim 1. Specifically, Miller **does not teach or disclose** "a packet bus switch unit implemented on said integrated circuit chip coupled to receive said plurality of upstream packet transactions on an internal point-to-point packet bus link and configured to determine a destination of each of said plurality of upstream packet transactions." In addition Miller **does not teach or disclose** "wherein said packet bus switch unit is further configured to route selected ones of said plurality of upstream packet transactions to **a first processor interface** coupled to **a first point-to-point packet bus link** and to route others of said plurality of upstream packet transactions to **a second processor interface** coupled to **a second point-to-point packet bus link** in response to determining said destination each of said plurality of upstream packet transactions" as recited in Applicant's claim 1.

Additionally, in regard to claim 17 and claim 18, the Examiner asserts that Miller teaches "a transceiver unit coupled to receive the selected ones of the plurality of upstream packet transactions and to transmit the selected ones of the plurality of upstream packet transactions on the point packet bus link." The Applicant respectfully disagrees with the Examiners assertion.

Specifically, as shown above, Miller teaches receiving upstream **(non-packet)** PCI level interrupts, transforming the interrupts into write packets and transmitting those

write packets upstream on one packet based interconnect. The Applicant asserts that this is not the same as "a first transceiver unit coupled to receive said selected ones of said of said plurality of upstream packet transactions and to transmit said selected ones of said of said plurality of upstream packet transactions on said first point to point packet bus link" and "a second transceiver unit coupled to receive said others of said plurality of upstream packet transactions and to transmit said others of said of said plurality of upstream packet transactions on said second point-to-point packet bus link" as recited in Applicant's claims 17 and 18, respectively.

Accordingly, the Applicant submits that claim 1, along with its dependent claims, patentably distinguishes over Miller for the reasons given above.

Furthermore, Applicant's claim 16 recites

> "A multiprocessor computer system comprising:
> a first processor and a second processor each configured to execute programmed instructions;
> an input/output node switch implemented on an integrated circuit chip **coupled to said first processor by a first point-to-point packet bus link** and **coupled to said second processor by a second point-to-point packet bus link,** wherein said input/output node switch includes:
> a bridge unit coupled to receive a plurality of peripheral transactions from a peripheral bus and configured to transmit a plurality of upstream packet transactions corresponding to said plurality of peripheral transactions;
> **a packet bus switch unit** coupled to receive said plurality of upstream packet transactions on an internal point-to-point packet bus link and configured to determine a destination of each of said plurality of upstream packet transactions;
> wherein said packet bus switch unit is further configured to **route selected ones of said plurality of upstream packet transactions to a said first processor via said first point-to-point packet bus link** and to **route others of said plurality of upstream packet transactions to said second processor via said second point-to-point packet bus link** in response to determining said destination each of said plurality of upstream packet transactions." (Emphasis added)

The Applicant submits that these features are likewise not taught or disclosed by Miller.

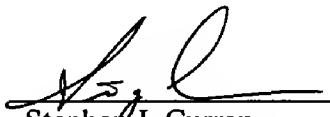
Accordingly, the Applicant submits that claim 16, along with its dependent claims, patentably distinguishes over Miller for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-73700/SJC.

Respectfully submitted,



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